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WHAT IS CLAIMED IS:

1. A synthesizer for generating signals to be input to successive mixers for modulating or demodulating an input signal $x(t)$, said synthesizer comprising: a first signal generator for producing a first ~~time-varying~~mixing signal ϕ_1 which varies irregularly over time; and a second signal generator for producing a second ~~time-varying~~mixing signal ϕ_2 which varies irregularly over time; where $\phi_1 * \phi_2$ has significant power at the frequency of a local oscillator signal being emulated, and neither ϕ_1 nor ϕ_2 has significant power at the frequency of said local oscillator signal being emulated.
2. The synthesizer of claim 1, wherein signals used to generate ϕ_1 and ϕ_2 do not have a significant amount of power at the output frequency of said output signal $x(t)$ $\phi_1 \phi_2$.
3. The synthesizer of claim 2, wherein $\phi_1 * \phi_1 * \phi_2$ does not have a significant amount of power within the bandwidth of said output signal $x(t)$ $\phi_1 \phi_2$.
4. The synthesizer of claim 3, wherein $\phi_2 * \phi_2$ does not have a significant amount of power within the bandwidth of said output signal $x(t)$ $\phi_1 \phi_2$.
5. The synthesizer of claim 4, wherein said first and second ~~time-varying~~mixing signals ϕ_1 and ϕ_2 are irregulargenerating using a single time base.
6. The synthesizer of claim 4, wherein said first and second ~~time-varying~~mixing signals ϕ_1 and ϕ_2 are digital waveforms.
7. The synthesizer of claim 4, wherein said first and second ~~time-varying~~mixing signals ϕ_1 and ϕ_2 are square waveforms.
8. The synthesizer of claim 4, wherein said first and second ~~time-varying~~mixing signals ϕ_1 and ϕ_2 are randomly generated.
9. The synthesizer of claim 4, wherein said first and second ~~time-varying~~mixing signals ϕ_1 and ϕ_2 are pseudo-randomly generated.

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10. The synthesizer of claim 4, wherein said first and second ~~time-varying~~mixing signals ϕ_1 and ϕ_2 are periodic functions of time.
11. The synthesizer of claim 4, wherein said first and second signal generators comprise:
pulse removal means for removing pulses from a local oscillator signal which has a frequency of twice the RF carrier, generating said first ~~time-varying~~mixing signal ϕ_1 ; and
complementary means for generating said second ~~time-varying~~mixing signal ϕ_2 .
12. The synthesizer of claim 4, wherein said pulse removal means comprises:
a pulse swallower for receiving an oscillator signal at twice the frequency of the local oscillator signal being emulated, and swallowing each pulse with a control signal S; and
a divide by two circuit for receiving and dividing said pulse swallowed signal by two, producing said first ~~time-varying~~mixing signal ϕ_1 .
13. The synthesizer of claim 12, wherein said complementary means comprises:
a delay circuit for receiving and delaying said control signal S to be synchronized in time with said first ~~time-varying~~mixing signal ϕ_1 , outputting said delayed control signal S as said second ~~time-varying~~mixing signal ϕ_2 .
14. The synthesizer of claim 4, wherein said first and second signal generators comprise:
shift register means for generating said first and second ~~time-varying~~mixing signals ϕ_1 and ϕ_2 by shifting out corresponding predetermined sequences.
15. The synthesizer of claim 14, wherein said shift register means comprises:
a shift register for receiving an oscillator signal at twice the frequency of the local oscillator signal being emulated, and generating said first ~~time-varying~~mixing signal ϕ_1 , by shifting out a predetermined sequence.
16. The synthesizer of claim 15, wherein said second signal generator comprises:

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an exclusive-OR (XOR) circuit for comparing outputs of consecutive latches in said shift register; and
a second shift register being clocked by said XOR output, and generating said second ~~time-varying~~mixing signal ϕ_2 , by shifting out a second predetermined sequence.

17. The synthesizer of claim 15, wherein said second signal generator comprises:

a third shift register for receiving said oscillator signal at twice the frequency of the local oscillator signal being emulated, and generating said second ~~time-varying~~mixing signal ϕ_2 , by shifting out a predetermined sequence.

18. The synthesizer of claim 4, wherein said first and second signal generators comprise:

means for generating said first ~~time-varying~~mixing signal ϕ_1 from an oscillator signal at the frequency of the local oscillator signal being emulated, and a control signal S having edges aligned with said oscillator signal; and
means for delaying said control signal S to produce said second ~~time-varying~~mixing signal ϕ_2 .

19. The synthesizer of claim 18, wherein said means for delaying comprises:
a delay latch for sampling said control signal S at the frequency of the local oscillator signal being emulated; and
an inverter for receiving and inverting said delay latched control signal S to produce said second ~~time-varying~~mixing signal ϕ_2 .

20. The synthesizer of claim 19, wherein said means for generating said first ~~time-varying~~mixing signal ϕ_1 comprises:

a second inverter for receiving the oscillator signal at the frequency of the local oscillator signal being emulated; and
an exclusive-OR (XOR) circuit for comparing said inverted oscillator signal with said latched input signal $x(t)$, producing said first ~~time-varying~~mixing signal ϕ_1 .

21. The synthesizer of claim 4, wherein said first signal generator comprises:
a shift register with a feedback loop.

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22. The synthesizer of claim 21, wherein said first signal generator comprises:
a shift register for receiving an oscillator signal at twice the frequency of the local oscillator signal being emulated, and generating said first ~~time-varying~~mixing signal ϕ_1 , by shifting out a predetermined sequence; and
a modulo-2 multiplier for receiving said first ~~time-varying~~mixing signal ϕ_1 and the output of an earlier latch in said shift register, feeding an output into a later latch in said shift register.

23. The synthesizer of claim 4 comprising:
one or more additional signal generators for producing one or more additional ~~time-varying~~mixing signals, varying irregularly over time;
where the product of all of said ~~time-varying~~mixing signals has significant power at the frequency of a local oscillator signal being emulated, and none of said all of said ~~time-varying~~mixing signals has significant power at the frequency of said local oscillator signal being emulated.

24. The synthesizer of claim 4, where said first signal generator comprises:
a divide by 2 circuit for receiving an oscillator signal at the frequency of the local oscillator signal being emulated; and
a divide by 4 circuit for receiving said oscillator signal at the frequency of the local oscillator signal being emulated;
selector means for routing either the output of said divide by 2 circuit or said divide by 4 circuit to an output, said output producing said first ~~time-varying~~mixing signal ϕ_1 .

25. The synthesizer ~~of any one of claims 12, 13, 18, 19 or 240~~, wherein said control signal S comprises a random signal.

26. The synthesizer ~~of any one of claims 12, 13, 18, 19 or 240~~, wherein said control signal S comprises a pseudo-random signal.

27. The synthesizer ~~of any one of claims 12, 13, 18, 19 or 240~~, wherein said control signal S comprises a periodic signal.

28. The synthesizer ~~of any one of claims 12, 13, 18, 19 or 240~~, comprising:

a delta-sigma (~~i.e.~~ Δ -S) modulator for generating said control signal S.

29. The synthesizer of claim 4 comprising:

first and second latches which are clocked via a common clock, to align said first and second ~~time-varying~~ mixing signals ϕ_1 and ϕ_2 .

30. An integrated circuit comprising the synthesizer of ~~any one of claims 1-29~~ claim 1.

~~31. A computer readable memory medium, storing computer software code in a hardware development language for fabrication of an integrated circuit comprising the synthesizer of any one of claims 1-29.~~

~~32. A computer data signal embodied in a output wave, said computer data signal comprising computer software code in a hardware development language for fabrication of an integrated circuit comprising the radio transmitter of any one of claims 1-29.~~

33. The synthesizer of claim 4, wherein the patterns of said first and second mixing signals ϕ_1 and ϕ_2 are different from one another.